CLAIMS

1. A teacher-pupil flip-flop, comprising:

a teacher circuit, comprising:

a gate circuit, having an output and having a plurality of inputs coupled to an intermediate node pair and receiving a clock signal, that switches after a setup delay in response to transitions of said clock signal between first and second states;

a stack circuit, coupled to said gate circuit output and to an input data node, that switches said intermediate node pair to a preliminary state after said setup delay when said clock signal transitions to said first state, and that switches said intermediate node pair to a data state indicative of said input data node after said setup delay when said clock signal transitions to said second state;

a keeper circuit coupled to said intermediate node pair; and

a teacher output circuit, coupled to said intermediate node pair, that drives an output node indicative of said data state; and

a pupil circuit, comprising:

a latch circuit, coupled to said intermediate node pair, that stores said data state of said intermediate node pair; and

a pupil output circuit, coupled to said latch circuit and receiving said clock signal, that drives said output node indicative of said data state after said clock signal transitions to said first state.

2. The teacher-pupil flip-flop of claim 1, further comprising:

said intermediate node pair including a pull-up node and a pull-down node; and

said stack circuit comprising:

a first stack circuit that drives said pull-down node low during said preliminary state, and that drives said pull-down node high during said data state if said input data node is low upon expiration of said setup time delay; and

a second stack circuit that drives said pull-up node high during said preliminary state, and that drives said pull-up node low during said data state if said input data node is high upon expiration of said setup time delay.

3. The teacher-pupil flip-flop of claim 2, wherein said teacher output circuit comprises:

an output P-channel device having a source coupled to a voltage supply, a gate coupled to said pull-up node and a drain coupled to said output node; and

an output N-channel device having a source coupled to ground, a gate coupled to said pull-down node and a drain coupled to said output node.

4. The teacher-pupil flip-flop of claim 3, wherein said output P-channel device tri-states its drain while said pull-up node is high, and wherein said output N-channel device tri-states its drain while said pull-down node is low.

5. The teacher-pupil flip-flop of claim 2, wherein said gate circuit comprises:

a NAND gate having a first input receiving said clock signal, a second input coupled to said pull-up node and an output coupled to said stack circuit; and

a NOR gate having a first input receiving an inverted clock signal, a second input coupled to said pull-down node and an output coupled to said stack circuit.

6. The teacher-pupil flip-flop of claim 5, wherein:

said first stack circuit comprises:

a first stack P-channel device having a source coupled to a voltage supply, a gate coupled to said output of said NAND gate and a drain;

a second stack P-channel device having a source coupled to said drain of said first stack P-channel device, a gate coupled to said data input node and a drain coupled to said pull-down node; and

a first stack N-channel device having a drain coupled to said pull-down node, a gate coupled to said output of said NAND gate and a source coupled to ground; and

wherein said second stack circuit comprises:

a third stack P-channel device having a source coupled to said voltage supply, a gate coupled to said output of said NOR gate and a drain coupled to said pull-up node;

a second stack N-channel device having a drain coupled to said pull-up node, a gate coupled to said data input node and a source; and

a third stack N-channel device having a drain coupled to said source of said second stack N-channel device, a gate coupled to said output of said NOR gate and a source coupled to ground.

7. The teacher-pupil flip-flop of claim 2, wherein said keeper circuit comprises:

a pull-up keeper circuit, comprising:

a first inverter having an input coupled to said pull-up node of said intermediate node pair and an output; and

a pull-up N-channel device having a drain coupled to said pull-up node, a gate coupled to said output of said first inverter and a source coupled to ground; and

a pull-down keeper circuit, comprising:

a second inverter having an input coupled to said pull-down node of said intermediate node pair and an output; and

a pull-down P-channel device having a source coupled to a voltage source, a gate coupled to said output of said second inverter and a drain coupled to said pull-down node.

8. The teacher-pupil flip-flop of claim 2, wherein said latch circuit comprises:

a pass P-channel device having a source coupled to a voltage source, a gate coupled to said pull-up node and a drain coupled to a data storage node;

a pass N-channel device having a drain coupled to said data storage node, a gate coupled to said pull-down node and a source coupled to ground;

a first inverter having an input coupled to said data storage node and an output coupled to an inverted data storage node; and

a second inverter having an input coupled to said inverted data storage node and an output coupled to said data storage node.

9. The teacher-pupil flip-flop of claim 8, wherein said pupil output circuit comprises:

a first P-channel device having a source coupled to said voltage source, a gate receiving an inverted clock signal and a source coupled to a feedback pull-up node;

a first N-channel device having a drain coupled to said feedback pull-up node, a gate receiving said inverted clock signal and a source coupled to said inverted data storage node;

a second P-channel device having a source coupled to said inverted data storage node, a gate receiving said clock signal and a drain coupled to a feedback pull-down node;

a second N-channel device having a drain coupled to said feedback pull-down node, a gate receiving said clock signal and a source coupled to ground;

an output P-channel device having a source coupled to said voltage source, a gate coupled to said feedback pull-up node and a drain coupled to said output node; and

an output N-channel device having a source coupled to ground, a gate coupled to said feedback pull-down node and a drain coupled to said output node.

10. The teacher-pupil flip-flop of claim 9, wherein said output P-channel device tri-states its drain while said feedback pull-up node is high, and wherein said output N-channel device tri-states its drain while said feedback pull-down node is low.

11. A register, comprising:

a first gate having a first input receiving a clock signal, a second input coupled to a pull-up node and an output;

a second gate having a first input receiving an inverted clock signal, a second input coupled to a pull-down node and an output;

a first stack circuit having a first input coupled to said first gate output, a second input coupled to a data input and an output coupled to said pull-down node;

a second stack circuit having a first input coupled to said second gate output, a second input coupled to said data input and an output coupled to said pull-up node;

a first keeper circuit coupled to said pull-down node;

a second keeper circuit coupled to said pull-up node;

a first output circuit comprising complementary devices having inputs coupled to said pull-down and pull-up nodes and outputs coupled to an output node;

a storage circuit having a first input coupled to said pull-down node, a second input coupled to said pull-up node, and at least one storage node; and

a second output circuit, receiving said clock and inverted clock signals, having an input coupled to said at least one storage node of said storage circuit, and having complementary output devices coupled to said output node.

12. The register of claim 11, wherein said first gate is a NAND gate and wherein said second gate is a NOR gate.

13. The register of claim 11, wherein:

said first stack circuit comprises:

a first P-channel device having a source coupled to a voltage supply, a gate coupled to said first gate output and a drain;

a second P-channel device having a source coupled to said drain of said first P-channel device, a gate coupled to said data input and a drain coupled to said pull-down node; and

a first N-channel device having a drain coupled to said pull-down node, a gate coupled to said first gate output and a source coupled to ground; and

wherein said second stack circuit comprises:

a third P-channel device having a source coupled to said voltage supply, a gate coupled to said second gate output and a drain coupled to said pull-up node;

a second N-channel device having a drain coupled to said pull-up node, a gate coupled to said data input and a source; and

a third N-channel device having a drain coupled to said source of said second N-channel device, a gate coupled to said second gate output and a source coupled to ground.

14. The register of claim 11, wherein said first output circuit comprises:

a P-channel device having a source coupled to a voltage source, a gate coupled to said pull-up node and a drain coupled to said output node; and

an N-channel device having a source coupled to ground, a gate coupled to said pull-down node and a drain coupled to said output node.

15. The register of claim 11, wherein said storage circuit comprises:

a P-channel pass device having a source coupled to a voltage source, a gate coupled to said pull-up node and a drain coupled to a storage node;

an N-channel pass device having a source coupled to ground, a gate coupled to said pull-down node and a drain coupled to said storage node;

a first inverter having an input coupled to said storage node and an output coupled to an inverted storage node; and

a second inverter having an input coupled to said inverted storage node and an output coupled to said storage node.

16. The register of claim 11, wherein said second output circuit comprises:

a first P-channel device having a source coupled to a voltage source, a gate receiving said inverted clock signal and a drain;

a first N-channel device having a drain coupled to said drain of said first P-channel device, a gate receiving said inverted clock signal and a source coupled to said at least one storage node of said storage circuit;

a second P-channel device having a source coupled to said at least one storage node of said storage circuit, a gate receiving said clock signal and a drain;

a second N-channel device having a source coupled to ground, a gate receiving said clock signal and a drain coupled to said drain of said second P-channel device;

a third P-channel device having a source coupled to said voltage source, a gate coupled to said drain of said first P-channel device and a drain coupled to said output node; and

a third N-channel device having a source coupled to ground, a gate coupled to said drain of said second P-channel device and a drain coupled to said output node.

17. A register, comprising:

a gate circuit, having a plurality of inputs receiving a clock signal and coupled to first and second intermediate nodes, and having first and second outputs switched in response to said plurality of inputs after a delay;

a stack circuit, having first and second inputs respectively coupled to said first and second outputs of said gate circuit, having a third input coupled to a data input, and having first and second outputs respectively coupled to said first and second intermediate nodes;

wherein said gate and stack circuits are operative to toggle said first and second intermediate nodes between an initial state when said clock signal transitions low after said delay and a data state indicative of said data input when said clock signal transitions high after said delay;

a keeper circuit that latches said data state of said first and second intermediate nodes;

an output circuit that drives an output node with valid data while said first and second intermediate nodes are in said data state; and

a pupil circuit that stores said data state of said first and second intermediate nodes and that drives said output node with valid data while said clock signal is low.

18. The register of claim 17, wherein said gate circuit comprises a NAND gate and a NOR gate.

19. The register of claim 17, wherein said stack circuit comprises a plurality of N-channel and P-channel devices coupled in series between a voltage source and ground.

20. The register of claim 17, wherein said pupil circuit comprises a storage circuit that stores said data state of said first and second intermediate nodes and a second output circuit coupled to said storage circuit and said output node and receiving said clock signal.